

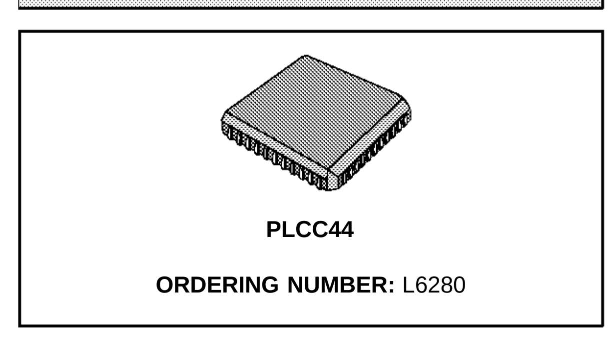
L6280

THREE CHANNELS MULTIPOWER DRIVER SYSTEM

ADVANCE DATA

- PROGRAMMABLE CONFIGURATION (CHANNELS 1 AND 2)
- OUTPUT CURRENT UP TO 1A (CHANNELS 1 AND 2)
- 1 SENSE PER CHANNEL
- OUTPUT CURRENT CHANNEL 3 UP TO 3A
- DIRECT INTERFACE TO MICROPROCESSOR
- C-MOS COMPATIBLE INPUT
- INTERNAL DC-DC CONVERTER FOR LOGIC SUPPLY (+5V)
- POWER FAIL
- WATCHDOG MANAGEMENT
- THERMAL PROTECTION
- VERY LOW DISSIPATED POWER (SUITABLE FOR USE IN BATTERY SUPPLIED APPLICATIONS)

MULTIPOWER BCD TECHNOLOGY



PLCC44

ORDERING NUMBER: L6280

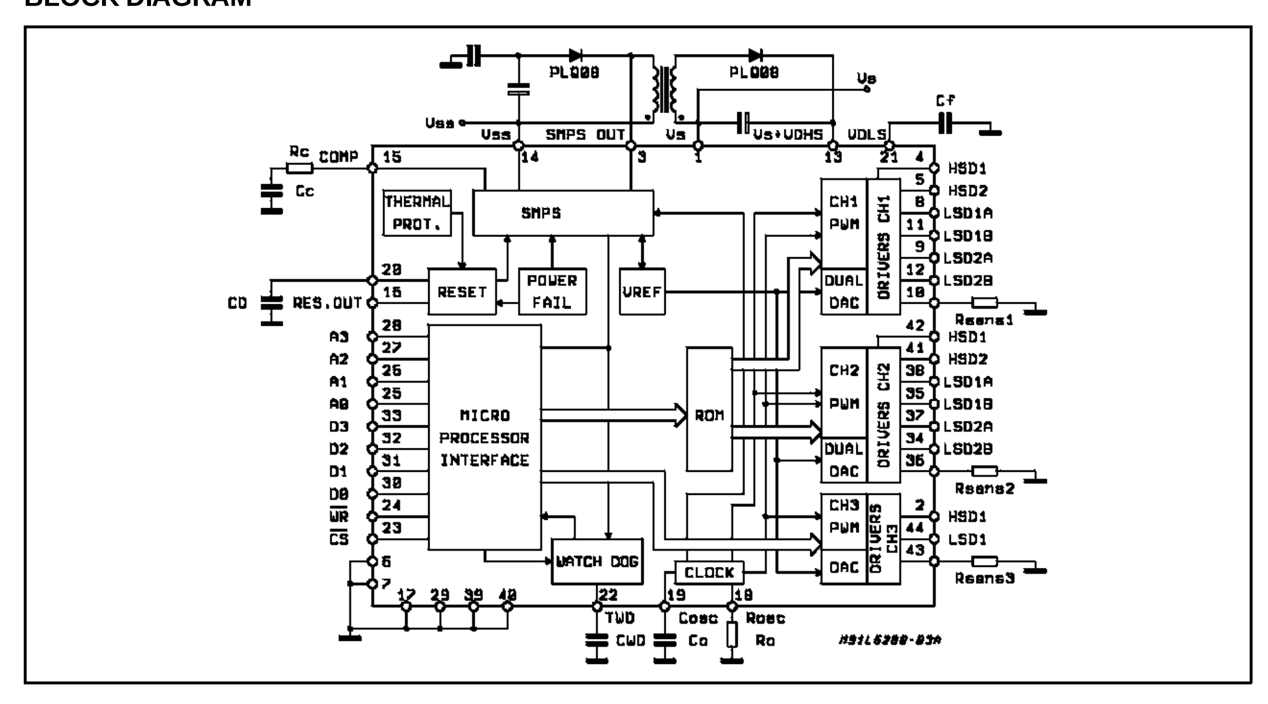
DESCRIPTION

The L6280 is a multipower driver system for motor and solenoid control applicatios that connects directly to a microprocessor bus. Realized in Multipower BCD technology -- which combines isolated DMOS transistors, CMOS & bipolar circuits on the same chip -- it integrates two 1A motor drivers (channels 1 & 2) a 3A solenoid driver (channel 3) and a 5V switchmode power supply.

All of the drivers in the L6280 are controlled by a microprocessor which loads commands and reads diagnostic information, treating the device as a peripheral. Channels 1 and 2 feature a programmable output DMOS transistor configuration that can be set during the initialization phase.

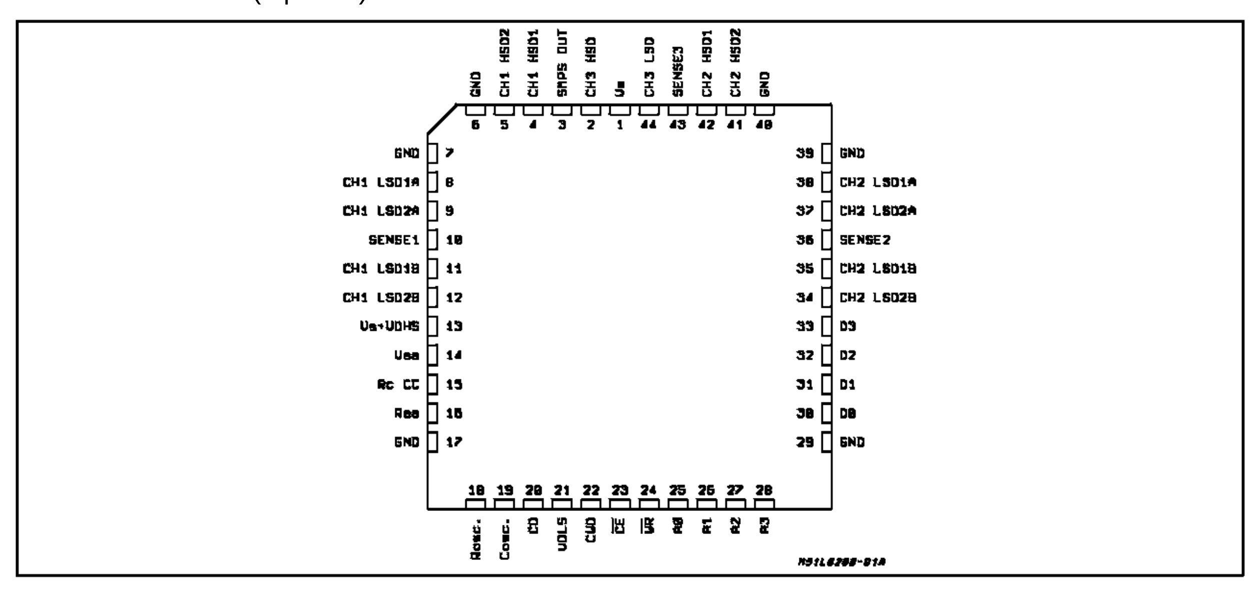
Thanks to very low dissipation of its DMOS power stages the L6280 needs no heatsink and is packaged in a 44-lead PLCC package.

BLOCK DIAGRAM



This is advanced information on a new product now in development or undergoing evaluation. Details are subject to change without notice.

PIN CONNECTION (top view)



ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	Value	Unit
V_S	Power Supply Voltage (Note A)	35	V
V_{SS}	Logic Supply Voltage	7	V
V13	Pin 13 Input Voltage (Note B)	60	V
V_{DHS}	High Side Out Transistor Driving Voltage (Note B,C)	18	V
V_O	Output Voltage. CH1; CH2: Unipolar Motor Drive (Note D) CH3	60 60	V V
V_{OD}	Differential Output Voltage CH1; CH2; Full Bridge Configuration (Note E)	60	V
V_{sense}	Sensing Voltage	-1 to 2	V
V_I	Logic Input Voltage	-0.3 to V_{SS} +0.3	V
I_{LSD}	Low Side Driver Input Current CH1; CH2 DC Operation Peak (Note F) CH3 DC Operation Peak (Note G)	 0.7 2 3 4.4	 A A A A
I_{HSD}	High Side Driver Onput Current CH1; CH2 DC Operation Peak (Note F) CH3 DC Operation Peak (Note G)	 1 2 3 4.4	 A A A A
I_{SSOUT}	SMPS Output Current (Continuous) (Peak; TON < 5ms)	1 2	A A
I_{RES}	Reset Output Open Drain Input Current	16	mA
P_{tot}	Total Power Dissipation atTamb = 70°C (Note H)	1.6	W
T_{stg}; T_j	Storage an Junction Temperature Range	-40 to 150	°C

Notes: A) D0 = D1 = D2 = D3 =0; B) V13 = V_S + V_{DHS}; C) At 20V > V_{DHS} > 17V the input current at pin 13 must be < 30mA; D) D0 = 1; D1 = D2 = D3 = 0; E) D1 = 1; D0 = X; D2 = D3 = 0; F) The pulse width must be < 5ms and the Duty Cycle must be < 10% G) The pulse width must be <5ms and the Duty Cycle must be < 6%; H) mounted on board with minimized dissipating copper area.

THERMAL DATA

Symbol	Description		Value	Unit
$R_{th\ j\text{-}pins}$ $R_{th\ j\text{-}amb}$	Thermal Resistance Junction-pins Thermal Resistance Junction-ambient (*)	Max. Max.	12 50	°C/W °C/W

(*) Mounted on board with minimized dissipating copper area.

PIN DESCRIPTION

PINS	NAME	FUNCTIONS
1	V_S	Power Supply Voltage Input
2	HSD 1	High Side CH 3 Power Output
3	SMPS OUT	Output of Switchmode Power Supply
4	HSD 1	High Side CH 1 Power Output
5	HSD 2	High Side CH 1 Power Output
6, 7,17,29, 39, 40	GND	Common Grounded Terminal
8	LSD 1A	Low Side CH 1 Power Output
9	LSD 2A	Low Side CH 1 Power Output
10	SENSE 1	A Resistor Rsense, connected to this pin allows load current control for CH 1
11	LSD 1B	Low Side CH 1 Power Output
12	LSD 2B	Low Side CH 1 Power Output
13	V_S +V_{DHS}	Input Voltage for the HSD Gates Drive
14	V_{SS}	Logic Supply Voltage Input
15	Comp.	An RC series network allows the compensation of the SMPS regulation loop
16	RES OUT	The reset open drain output can be used to warn the microprocessor about V_S and V_{SS} status
18	R_{OSC}	Together with C_{OSC}, sets the cycle time of the SMPS t = 1.1 $R_O C_O$
19	C_{OSC}	Together with C_{OSC}, sets the cycle time of the SMPS t = 1.1 $R_O C_O$ and sets the minimum ON time in the PWM current control loop
20	C_D	The value of this capacitor sets the reset delay $t_D = 7 \times 10^4 C_D$
21	V_{DLS}	By-pass Capacitor of the LSD Gates Voltage drive
22	t_{WD}	The value of this CWD sets the duration of the watchdog monostable $t_{WD} = 3 \times 10^4 C_{WD}$. If no watchdog signal is generated into the TWD time the device is automatically switched off.
23	$\overline{CS}$	Enable Input (active when low)
24	$\overline{WR}$	Write Input. When $\overline{WR}$ is low the data is loaded into the µP interface
25	A0	Operation Selection (see programming sequence).
26	A1	Operation Selection (see programming sequence).
27	A2	Channel Selection (see programming sequence).
28	A3	Channel Selection (see programming sequence).
30	D0	Data (see programming sequence).
31	D1	Data (see programming sequence).
32	D2	Data (see programming sequence).
33	D3	Data (see programming sequence).
34	LSD 2B	Low Side CH 2 Power Output
35	LSD 1B	Low Side CH 2 Power Output
36	SENSE 2	A Resistor R_{sense}, connected to this pin allows load current control for CH 2
37	LSD 2A	Low Side CH 2 Power Output
38	LSD 1A	Low Side CH 2 Power Output
41	HSD 2	High Side CH 2 Power Output
42	HSD 1	High Side CH 2 Power Output
43	SENSE 3	A Resistor R_{sense}, connected to this pin allows load current control for CH 3
44	LSD 1	Low Side CH 3 Power Output

ELECTRICAL CHARACTERISTICS (V_S = 20V; T_j = 25°C; V_{SS} = 5V; V_{DHS} =15V; R_O =165KΩ; C_O =680pF; unless otherwise specified)

Symbol	Parameter	Test Condition	Min.	Typ.	Max.	Unit
I_{DSS}	Leakage Current	Fig. 1 V_{DS} = 60V			2	mA
V_s	Power Supply Voltage	Note 1,2	>V_{PF}		48	V
V_{INL}	Low Level Input Voltage		-0.3		1.35	V
I_{INL}	Low Level Input Current				-10	µA
V_{INH}	High Level Input Voltage		3.15		V_{SS}	V
I_{INH}	High Level Input Current				10	µA
V_{ROUT}	Low Level Reset Out	I16 = 1.5mA			0.8	V
V_{PF}	Power Supply Fail Voltage	(Fig. 2)			13	V
I_S	Quiescent Supply Current	V_S = 12V	4.5	6	7.5	mA
V_{SS}	Logic Supply Voltage		4.75	5	5.25	V
$I_{SS(IN)}$	Logic Supply Current		4.5	6	7.5	mA
$I_{SS(OUT)}$	SMPS Out Current Range	Note 3			800	mA
f_{osc}	Oscillator Frequency		64	80	96	KHz
f_1	SMPS and CH3 Frequency			f_{osc}		KHz
f_{1max}	Max SMPS Switching Frequency				120	KHz
f_2	PWM Frequency			fosc/2		KHz
f_3	High Side Driver Switching Frequency			fosc/4		KHz
TSD	Thermal Shutdown		125	150		°C
t_{WD}	Monostable Watchdog Time	CWD = 0.22µF (Note 4)		6.6		ms
t_D	Reset Delay Time	C_D = 0.22µF; Fig.2 (Note 5)		15.4		ms
R_{ON}	ON State Drain Resistance Transistor LSD CH1 - CH2 HSD CH1 - CH2 LSD CH3 HSD CH3 SMPS	Fig 3; 4ab		2 1.1 0.5 0.5 1	2.4 1.4 0.8 0.8 1.2	Ω Ω Ω Ω Ω
SENSE	Internal Sense LOW-Pass Filter			300	500	ns
V_{ref}	DAC Reference Voltage	D0=D1=D2 =1 (Table 1)		1		V
DAC	DAC Resolution (3 Bit)	(See Table 1)		Vref/8		V
t_C	Discarge Time of Cosc Capacitor (Minimum TON)	(Note 6)		0.4		µs
V_{DHS}	HSD Gates Voltage Drive		13	15	17	V
I_{DHS}	Pin 13 Overage Input Current			3		mA
$I_{SS\ (OUT)\ max}$	SMPS Overload Protection Current		1.2			A
V_{DLS}	Pin 21 Overage Input Voltage			12		V
V_{SSF}	Logic V_{SS} Fail Threshold Voltage	(Fig. 2)	2.6		4.1	V
$V_{FHSD\ (1;2)}$	Internal Clamp Diode Forward Voltage CH1/CH2	@ I_{DS} = 0.4A (Fig. 5)			1.2	V
V_{FLSD} (1AB;2AB)	Internal Clamp Diode Forward Voltage CH1/CH2	@ I_{DS} = 0.4A (Fig. 5)			1.4	V
V_{FHSD}	Internal Clamp Diode Forward Voltage CH3	@ I_{DS} = 1A (Fig. 5)			1.1	V

ELECTRICAL CHARACTERISTICS (continued)

Symbol	Parameter	Test Condition	Min.	Typ.	Max.	Unit
V_{FLSD}	Internal Clamp Diode Forward Volt. CH3	@ I_{DS} = 1A (Fig. 5)			1.1	V
t_{CW}	Chip Seletion to End of Write	(Fig. 6)	700			ns
t_{WPW}	Write Pulse Width	(Fig. 6)	700			ns
t_{SU}	Data Set-up Time	(Fig. 6)	700			ns
t_{DH}	Data Hold-up Time	(Fig. 6)	0			ns
t_{WC}	Write Cycle Time	(Fig. 6)	2.7			ms

Notes:

1) When driving a unipolar stepper motor the Power Supply Voltage must be lower than 24V.

2) A lower Supply Voltage than the Power Fail threshold disables the Step Down Power Supply (see Fig.2)

3) The minimum output current equals the half of the peak-to-peak current ripple

4) $t_{WD} \cong C_{WD} \times 1.5 / 50 \times 10^{-6}$ (sec)

5) $t_D \cong C_D \times 3.5 / 50 \times 10^{-6}$ (sec)

6) $t_C \cong C_{OSC} \times R_{int.}$ (sec); $R_{int.} = 600\Omega \pm 30\%$

Figure 1: Drain Lekage Current Equivalent Test Circuit . The Gate-to-Source Voltage VGS is below the Switch-Off Threshold.

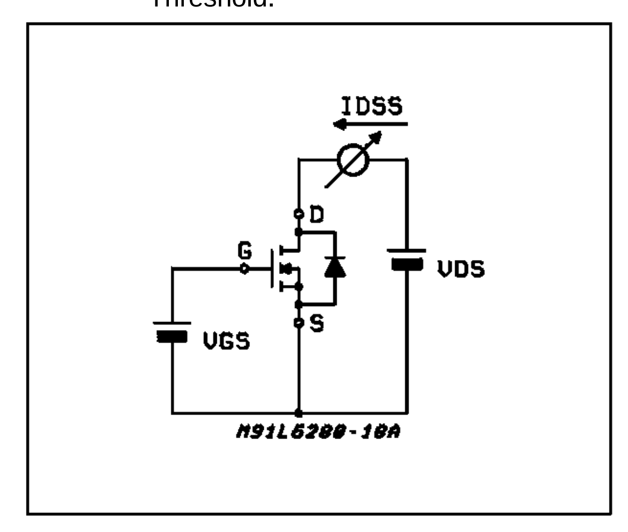


Figure 3: Typical Normalized $R_{DS(ON)}$ vs. Junction Temperature

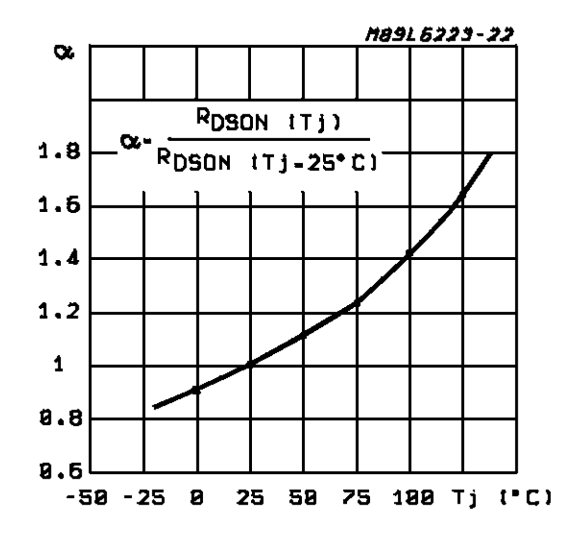


Figure 2: Reset Output Behaviour versus Power Supply Voltage V_S and/or Logic Supply Voltage V_{SS}.

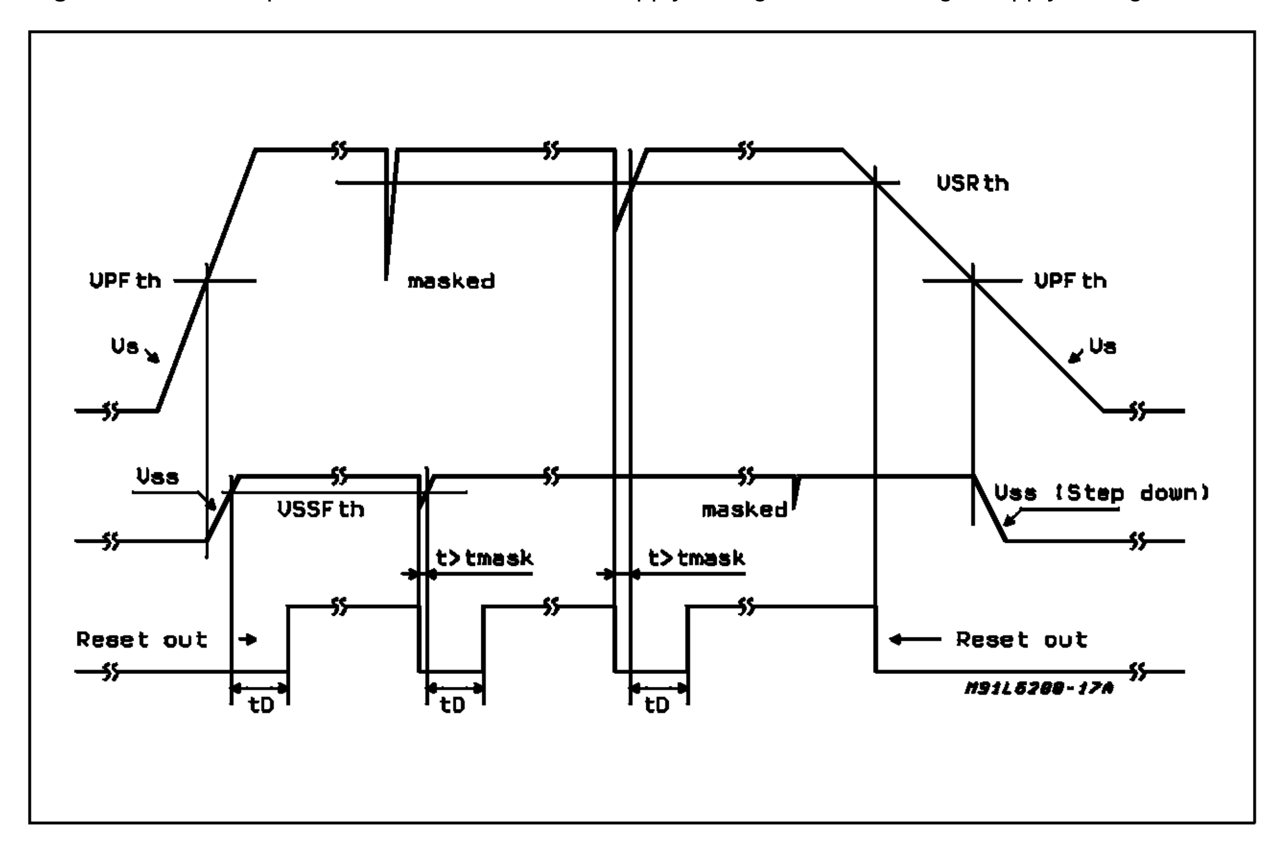


Figure 4a: Sink Output DMOS R_{ON} Equivalent Test Circuit

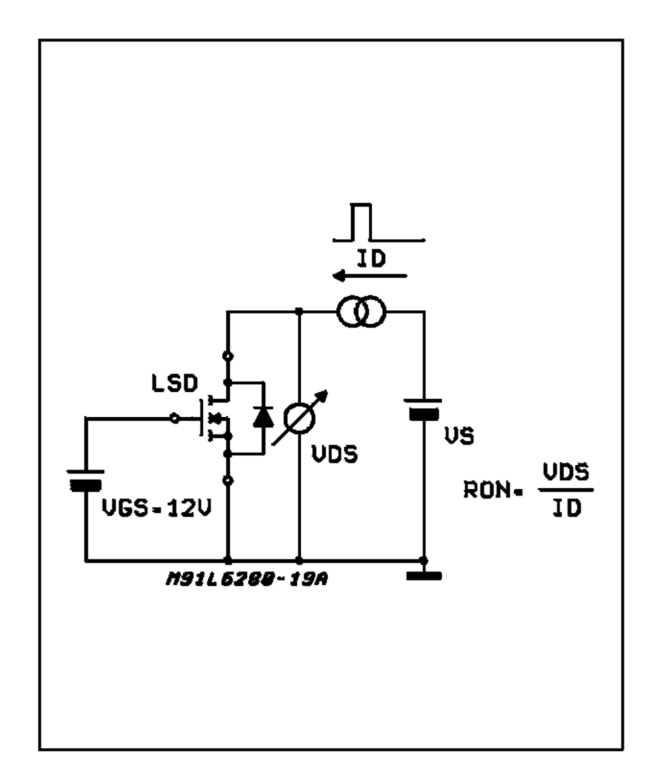


Figure 4b: Source Output DMOS R_{ON} Equivalent Test Circuit

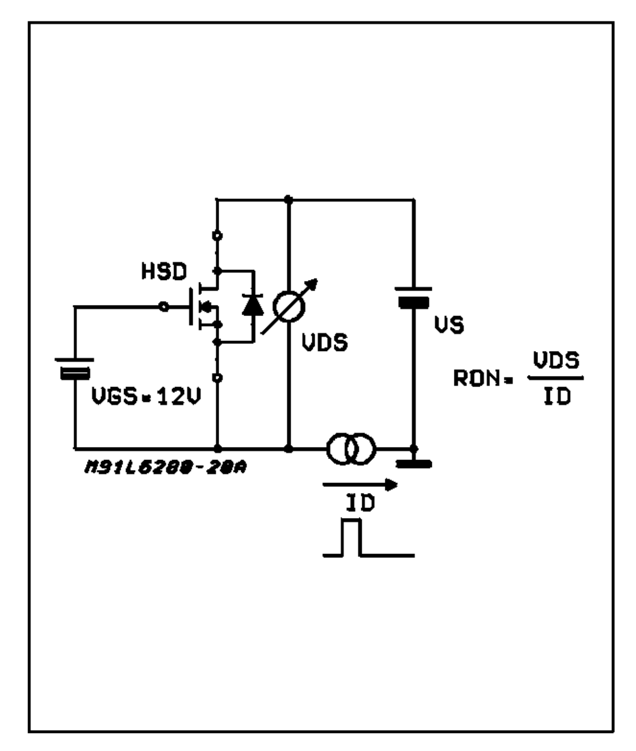
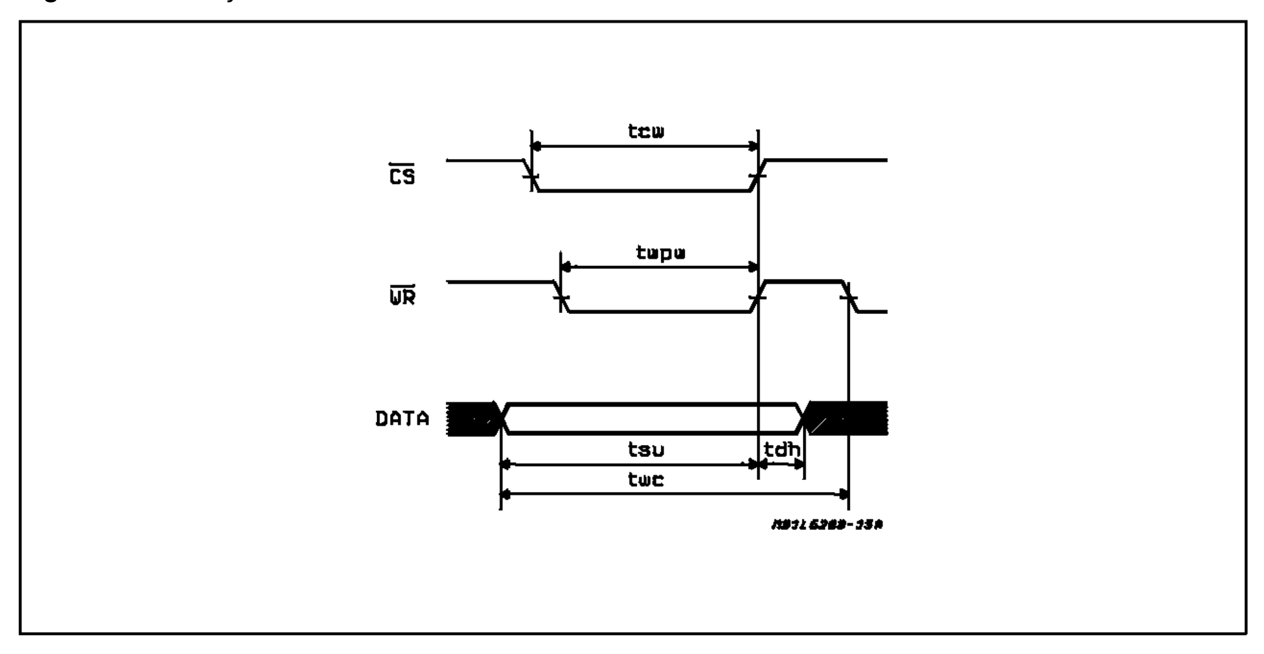


Figure 5: Possible Hardware Configurations of Power Stage (CH1 and CH2)

HSD1 HSD2
LSD1A LSD1B LSD2A LSD2B
Vs
UNIPOLAR STEPPER MOTOR
FULL BRIDGE
SOLENOID
DUAL HALF BRIDGE
DUAL SOLENOID

Figure 6: Write Cycle



SYSTEM DESCRIPTION (Refer to the Block Diagram)

The L6280 is a single chip power microsystem which includes drives for three different loads, the associated control logic and a Switched Mode Power Supply (SMPS) at $V_{SS} = 5V \pm 5\%$.

The IC can be directly connected to a standard microprocessor because of its common I/O interface architecture. The L6280 can exchange information regarding the load driver and the control method via a 8 bit data bus. The block named microprocessor interface decodes the first four bits (A0....A3), which, depending on the content of the remaining four (D0.......D3) are used to enable the power DMOS, to activate the PWM loop, and finally to set the D/A output value.

The power stage can be divided into 3 channels. Channels1 and 2 have 6 DMOS transistors each one (2high side drivers with $R_{dson} = 1\Omega$, 4 low side drivers with $R_{dson} = 2\Omega$). Depending on the application load, these driver transistors can be connected in different ways. The microprocessor, via software, must activate the proper control loop to optimize operation of different loads and output stage configurations. Because of this programmability in the control of the output configurations, a large variety of different loads can be driven by the same integrated circuit (see possible configuration for power stage on Figure 5) giving the greater system flexibility. Current levels up to 1A are possible from CH1 and CH2, limited primarily by the power dissipation of the IC.

The third channel has a fixed configuration intended to drive a solenoid. DMOS transistors with 0.5Ω R_{dson} are used to provide 4A max load capability.

All three channels have 3 bit current D/A resolution. Some auxiliary blocks of diagnostic and protection (e.g.: The power Fail/Reset and the watchdog) are provided to protect the system from microprocessor failure or power fail.

Step Down Switchmode Power Supply (See Figure 7).

The step down switchmode power supply contains a DMOS power stage with 1Ω R_{dson} (Q1), control circuitry, diagnostics and protection circuits; a regulated voltage ($V_{SSout)}$) is used to drive some of the internal circuit blocks and the external microprocessor and memories. Thanks to the DMOS output stage this regulator can deliver a continuous output power of 4W (5V; 0.8A) with an efficiency betler than 90% at a typical frequency of 80kHz.

The regulation loop uses a classical pulse width modulation circuit that includes a sawtooth generator, an error amplifier, a voltage comparator and a PWM latch. A precision 5V reference is generated and trimmed on chip to guarantee a 5% tolerance. This reference is used as voltage reference for the SMPS and the reference for the DACs.

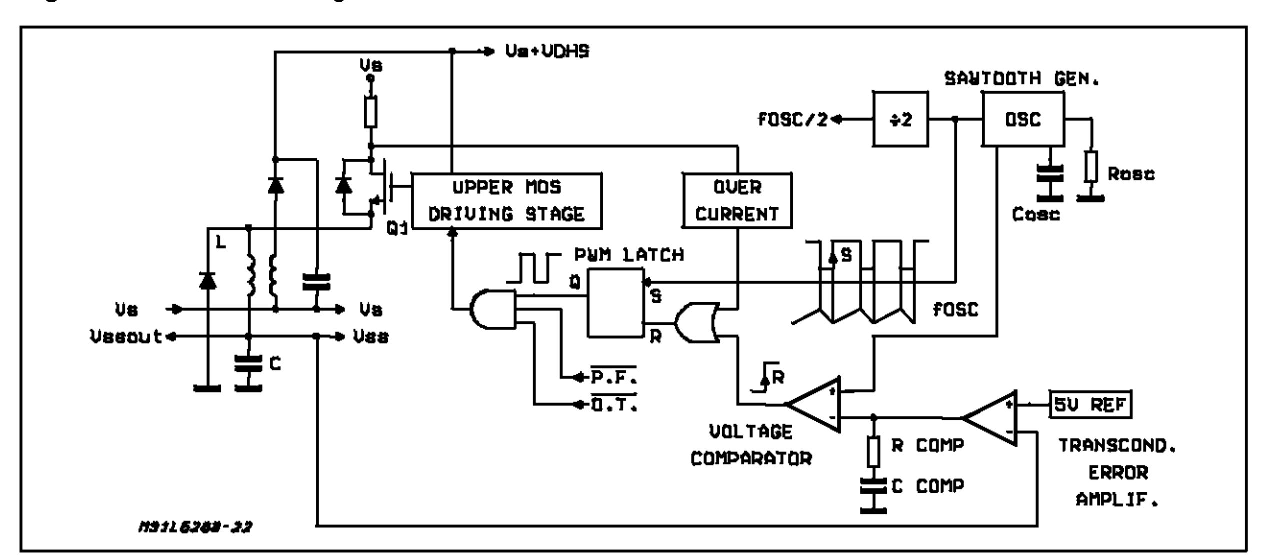
The IC also provides an extra voltage (V_S+V_{DHS}) for the correct driving of the high side drivers. These transistors require a gate voltage higher than the supply voltage Vs to obtain the minimum ON resistance. Because of the v ery low current needed to drive DMOS transistors, this auxiliary voltage is easily obtained from a second winding on the inductor of the LC output network (see Application Information).

An overcurrent protection circuit is included to turn OFF the power transistor when a current level of 1.2A is exceeded.

The SMPS block also includes a voltage sensing circuit to generate a power ON reset signal for the microprocessor. This Power Fail circuit senses the input supply voltage and the output regulated voltage and sets the Reset-out pin to the high voltage only when both the sensed voltages are correct.

Finally, the SMPS block is able to deliver $f_{OSC/2}$ used in the actuation stage for the PWM control of the current (CH1; CH2 and CH3).

Figure 7: SMPS Block Diagram



Pwm Current Control Loop

The current control is achieved big a cycle of charge (T_{ON}) and discharge (T_{OFF}) of the energy stored in each couple of windings of the driven motor (MA and MB). Fig. 8 shows the windings MA of an unipolar stepper motor during T_{ON}. FF1 is setted by the clock pulse and the transistor Q_A is ON. At the moment $Q_1$is ON the current exponentially increases until $R_S \times I_P$ equals V_{REF}.

A reset pulse is produced, Q_A is switched OFF and Q_2 is switched ON (Fig. 9). Since the magnetic flux $0_{MA} = N_A\ I_P$ cannot suddenly change and since the coil tourus number in the discharge loop is doubled, the peak current I_P modifies it self into $I_P/2$. The OFF time is characteryzed by a slow recirculation of the current $I_P/2$ that decreases until a new clock pulse sets a new T_{ON} configuration. To control the current in two separate windings MA and MB with just one sense resistor RS and one comparator, a special PWM control loop based on a ”time sharing” technique (Patented) is used (Fig. 10).

In this configuration the chopping frequency, that defines the $T_{ON} + T_{OFF}$ period of each phase, is halved by FF3 that drives ON G1 and G2 alternately. During T_{OFF} of one winding, for instance MA (and Q_A is OFF), its current does not flow throught the sensing resistor that can be used to monitor the current that flows through the second winding MB, allowed by the ON-status of Q_B.

Fig. 11 shows a simplified timing before and during the phase change from AB to $\overline{AB}$ (CCW, full step). It can be seen that before the time t_1, I_A and I_B are alternately controlled in a chopping period Tch1 of 4 oscillator periods or two clock periods. The time sharing is 50% - 50% and the chopping frequency is typically of 20KHz (f_{osc} = 80KHz).

Afther the time t_1, as soon as $I_{\overline{A}}$ is sensed, a different time sharing is generated. In fact since a Reset pulse is last after one clock pulse, FF2 can drive FF3 to change for I_B chopping only at the next clock pulse (Fig 10; Fig 11).

This means that the chopping time becomes Tch2 = 6 oscillator pulses, the frequency decreases to 16.6KHz (f_{osc} = 80 KHz) and the time sharing becomes of 67% - 33%.

At the end of the phase change period tphc the time sharing comes back to 50% - 50% again. It can be noted that this behaviour allows a faster phase change and then a higher speed of the motor. The cost of that, is the increase of the T_{OFF} of the unchanged phase B and then a small increase of the ripple of the current I_B (see $\Delta I_{B1} < \Delta I_{B2}$ in Fig. 11).

This time sharing current control method is also used when two indipendent load are driven by one single channel. when only one load is present, such as a DC motor could be, the time sharing is automatically switched OFF and the PWM frequency becomes $f_{osc}/4$ = 20KHz. Table 1 shows how the reference voltage can be modified with a three bits DAC to allow microstepping operations (see below).

Figure 8 - T_{ON} Configuration: Motor Windings MA (A; $\overline{A}$).

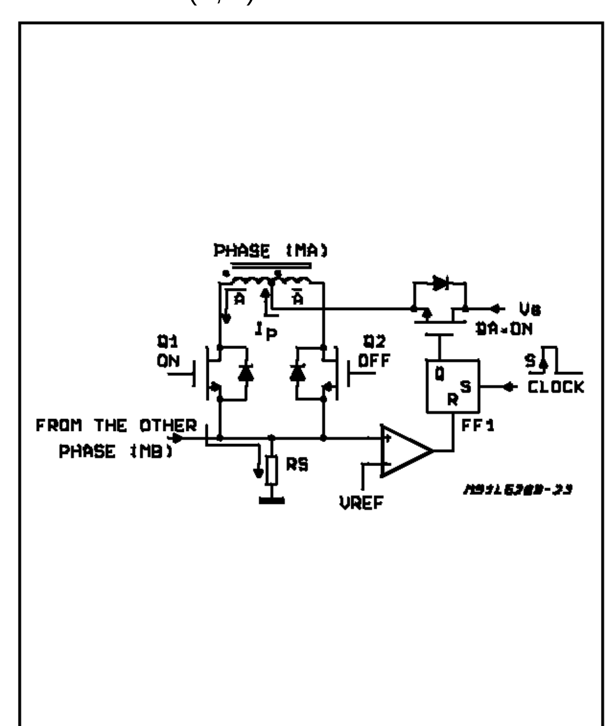
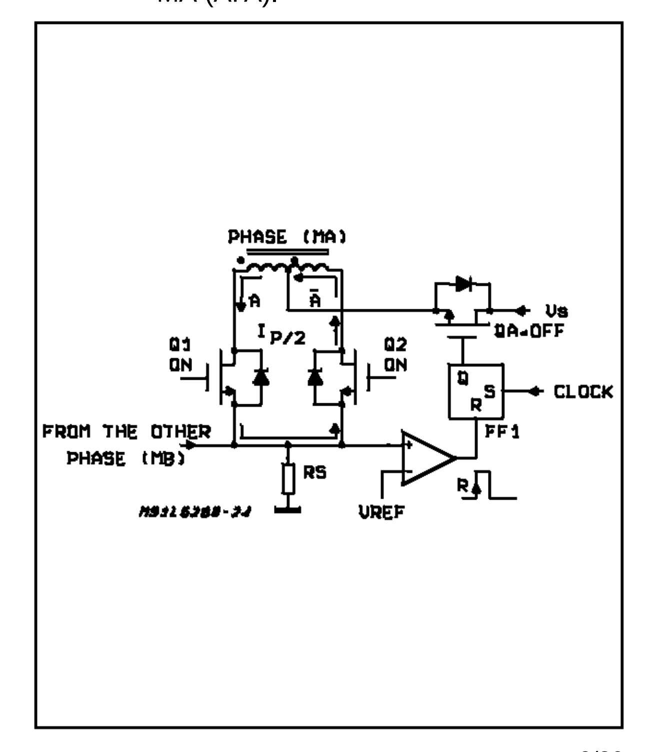


Figure 9 - T_{OFF} Configuration: Motor Windings MA (A: $\overline{A}$).



SGS-THOMSON MICROELECTRONICS

Figure 10 - PWM Current Control Loop. Time Sharing Technique.

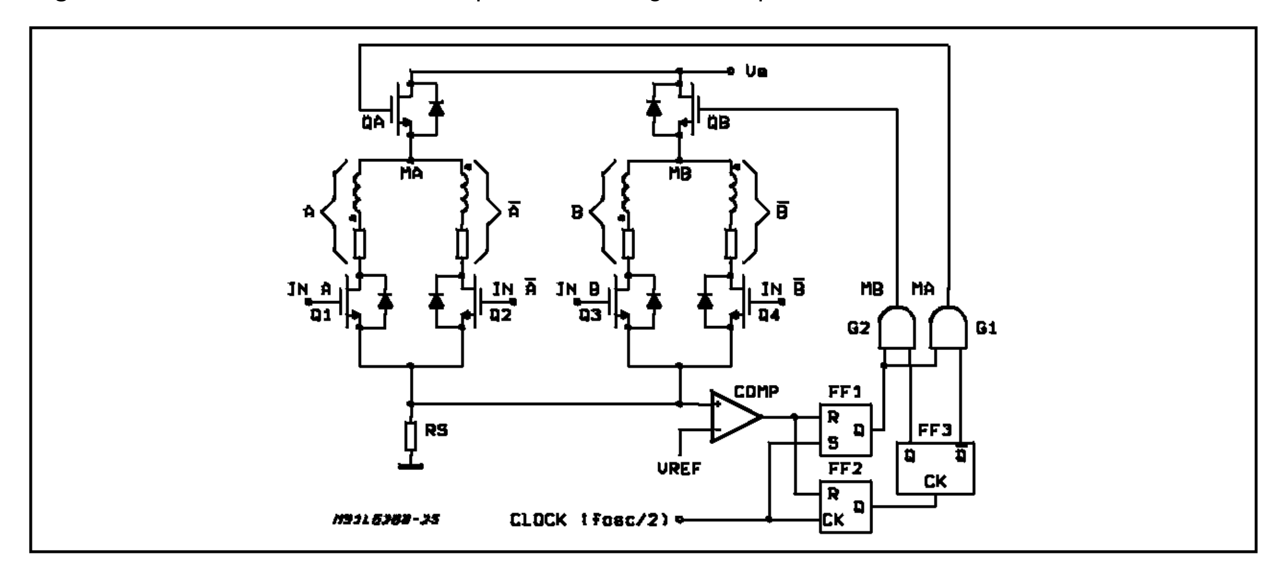


Figure 11: Chopping Characteristics (simplified)

Digital/Analog Converters (DACs)

The output current levels are programmed by 5DACs each with 3 bit resolution. Channels 1 and 2 each have 2 DACs, one for the left part of the output stage and the other for the right part. When the output stage is used to drive only one load (as with DC motors), the L6280 uses only the right register. Channel 3 has only 1 DAC.

Microstepping operation is easily performed with channels 1 and 2. The value of each DAC can be changed in two ways:

a) the new value can be directly generated by the microprocessor and then loaded into the specified DAC;

b) the value of a DAC can be incremented or decremented by 1; in this case the microprocessor during acceleration or deceleration has only to indicate the DAC on which operate and the type of the operation, reducing the CPU's burden.

The correspondence between the DAC value and the Vref level is shown in table 1.

Table 1

D2	D1	D0	V_{ref}	UNIT
1	1	1	1	V
1	1	0	0.875	V
1	0	1	0.75	V
1	0	0	0.625	V
0	1	1	0.5	V
0	1	0	0.375	V
0	0	1	0.25	V
0	0	0	0.125	V

Iload = 0 is obtained by disabling all low-side drivers.

Turn ON/OFF Characteristics and Program Sequence

During power-on the Switchmode Power Supply output stage is turned OFF till V_S reaches V_{PFth}. The pin Reset Out is held low and remains low till V_{SS} is < V_{SSFth} (the power stages and the logic of the L6280 are disabled.

Not correct signals coming from the microprocessor are then ignored; the microprocessor on the other hand, receives a low state signal from the Reset Out pin. When the V_{SS} output is stabilized during a delay t_D set by the C_D capacitor, the pin Reset Out goes to the high level; the microprocessor is enabled to work while the L6280 is in stand-by waiting for a keyword and initialization sequence. Every command that arrives before the keyword is ignored. At this time the programming sequence can start according to the flow diagram (Fig. 12).

At first the Keyword (00111010) has to be sent to the L6280 to activate the watch - dog function that begins to control the microprocessor functionality. From this moment the microprocessor must send periodically the Watch-dog word (00110101) otherwise its absence is interpreted as a microprocessor failure: to prevent any damage both in the load and in the IC, the L6280 itself disables the power stages. No reset signal is generated towards the CPU; the system must restart the sequence from Power-ON.

The next step is to set the configuration of channel 1 and channel 2 output stages by the initialization word. The configuration can be chosen to fit in the load characteristics. To do this the microprocessor generates a word with A0, A1 = 0 and where A2, A3 choose the channel to be configured, D0 to D3 choose the type of configuration (unipolar, dual half bridge or full bridge; see Data and Address decoding). Every input configuration different from the allowed initialization word is ignored.

When the initialization arrives, the L6280 sets the configuration of the output stage of the chosen channel. The initialization word has to be repeated for the other channel (CH1 or CH2 only). If two initializations arrive for the same channel, the L6280 disables the output stages while pin Reset Out goes low for a time Td to advise the mocroprocessor about the uncorrect condition. The program sequence must restart from the Keyword step. After the initialization step is succesfully completed the L6280 begins to accept commands. If a command is sent before the relative channel has been configured, the command is neglected.

Command can be of three type:

a - selection of current level loading a DAC;

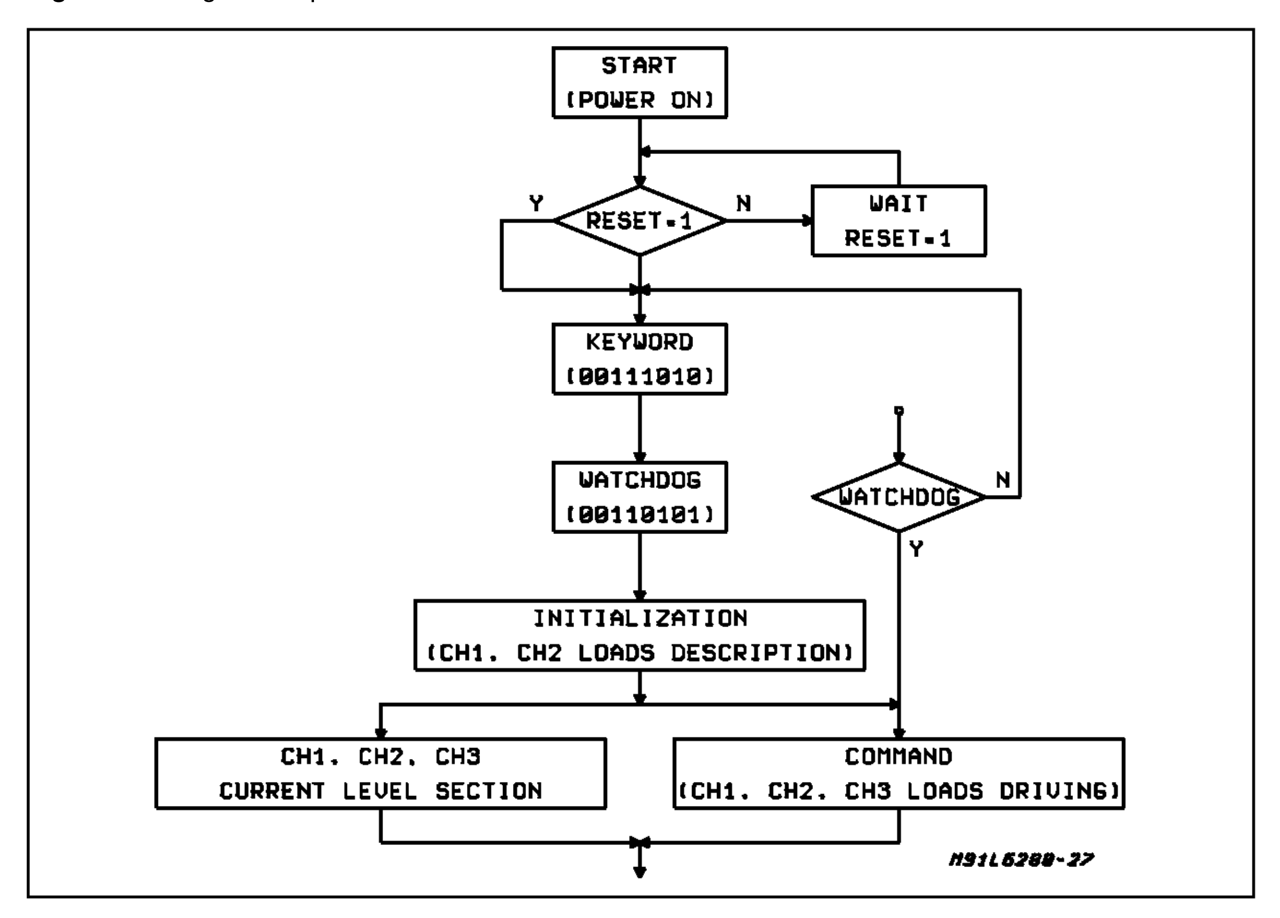
b - increment or decrement of a DAC;

c - selection of the driving strategy of a channel (e.g. half/full step, fast/slow decay and so on).

To select the current level is necessary to load a value into the appropriate DAC. The microprocessor must select the channel via A2, A3 and (only for channel 1 and 2) left or right DAC via D3; the value of D0,....D2 are loaded in the chosen DAC. There are two possibilities of changing the value of a DAC; the first one is to load directly the new value, the second one is to cause an increment or a decrement in a DAC, in this way the burden of the microprocessor can be partially decreased generating inc/dec command without calculating the value.

To increment od decrement a DAC the microprocessor must select the channel via A2,A3, left or right DAC and the operation via D0 to D3 according to truth table in Datas and Address Decoding (see below). The increment or decrement is done immediately after the arrive of the command. For every configuration of the output stages are possible different type of driving strategy explained in Datas and Address Decoding.

Figure 12: Program Sequence



Data and Address Decoding

SPECIAL WORDS

A3	A2	A1	A0	D3	D2	D1	D0
0	0	1	1	1	0	1	0

KEYWORD

This word is used during the start-up procedure to enable operations; all settings arrived before the keyword are reset.

A3	A2	A1	A0	D3	D2	D1	D0
0	0	1	1	0	1	0	1

WATCHDOG

The microprocessor must periodically generate this word; the value of the maximum period is set by the capacitor C_D. The absence of the Watchdog is interpreted by L6280 as a microprocessor failure. The maximum period is:

$$T_{WD} = C_D \times 1.5 / (50 \times 10E\text{-}6)$$

Except for special words (keyword and watchdog), the input words are organized like the following:

A0 A1 Operation selection

A2 A3 Channel selection

D0 D1 D2 D3 Datas

A0,A1 DECODING (OPERATION SELECTION)

A0,A1 select the type of operation (channel initialization, commands, DACs loading, DAC increment/decrement).

A0 A1

0 0 This configuration is used to send the information about the configuration of the vchannel specified by A3 and A2; D0 to D3 are used to specify the configuration of the channel (full bridge, dual half bridge, unipolar motor).

A0 A1

1 0 This configuration is used to change driving strategy of the output stages of the channel specified by A3 and A2 (full/half step, slow/fast decay and so on). The driving strategy is coded in D0 to D3, and depends from the configuration of the output stage.

A0 A1

0 1 This configuration is used to load the value of a DAC of the channel selected by A3 and A2. D3 indicates right and left DAC just for channel 1 and 2.

A0 A1
1 1 This configuration is used to cause an increment or a decrement of a DAC. Right or left DAC and inc/dec are selected by D0 to D3 value.

A2, A3 DECODING (Channel Selection)

Every time a command or a initialization is sent to the L6280, a channel must be selected. This is done via A2 and A3 according to the table.

A2	A3	
0	1	Select channel 2
1	0	Select channel 1
1	1	Select channel 3
0	0	Used only with keyword and watchdog

D0 to D3 DECODING (Datas)

The meaning of D0, D3 changes according to the value of A0, A1

A0 A1
0 0 When A0, A1 are in this configuration, and channel 1 or 2 is selected, the data appearing in D0 to D3 set the output power stage configuration to fit the chosed load according to the allowed Truth Table. There is no need to configure channel 3.

	D3	D2	D1	D0	Possible configurations for channels 1 and 2
	0	0	0	0	Null (power disabled)
a	0	0	0	1	Unipolar motor
b	0	0	1	0	Full Bridge
c	0	0	1	1	Dual Half Bridge

b) Full Bridge Configuration

a) Unipolar Motor Configuration

In this configuration D0 to D3 directly drive the low side drives:

D3	D2	D1	D0	Configurations	
0	0	0	0	Low side drivers 1,2,3,4 OFF	
0	0	0	1	Low side drivers 2,3,4 OFF	Low side driver 1 ON
0	0	1	0	Low side drivers 1,3,4 OFF	Low side driver 2 ON
0	1	0	0	Low side drivers 1,2,4 OFF	Low side driver 3 ON
0	1	0	1	Low side drivers 2,4 OFF	Low side drivers 1,3 ON
0	1	1	0	Low side drivers 1,4 OFF	Low side drivers 2,3 ON
1	0	0	0	Low side drivers 1,2,3 OFF	Low side driver 4 ON
1	0	0	1	Low side drivers 2,3 OFF	Low side drivers 1,4 ON
1	0	1	0	Low side drivers 1,3 OFF	Low side driver 2,4 ON

The following configurations are not allowed: the microprocessor does not to generate them otherwise they can cause faulty operations.

D3	D2	D1	D0	
0	0	1	1	Always not allowed
0	1	1	1	
1	0	1	1	
1	1	0	0	
1	1	0	1	
1	1	1	0	
1	1	1	1	This configuration is not allowed when driving a unipolar motor and it is permitted only to drive a high current solenoid.

In full bridge configuration D0 to D3 set the driving strategy of the bridge:

D0	D1	D2	D3	
X	0	0	0	Tristate left and right
X	0	0	1	Chopper left, brake right
X	0	1	0	Chopper right, brake left
X	0	1	1	Brake left, brake right
X	1	0	0	Tristate left and right
X	1	0	1	Diagonal chopper
X	1	1	0	Inverted diagonal chopper
X	1	1	1	Tristate left and right

c) Dual Half Bridge Configuration

D0	D1	D2	D3	
X	0	0	0	Tristate left and right
X	0	0	1	Brake right, chopper left
X	0	1	0	Brake right, chopper right
X	0	1	1	Brake left, brake right
X	1	0	0	Chopper left, chopper right
X	1	0	1	Tristate left, chopper right
X	1	1	0	Tristate right, chopper left
X	1	1	1	Tristate left and right

CHANNEL 3

For channel 3 only D0 has a meaning: it directly drives the low side driver DMOS. When D0 = 0 the low side driver DMOS is switched OFF and the current flows through external recirculation diodes.

A0 A1

1 0 When A0, A1 are in this configuration, D0 to D3 are used to set the strategy of the output power stages according to the output stage configuration previously selected.

A1 A0

1 0 When A0, A1 are in this configuration, D0 to D2 are loaded into left or right winding D/A converter, according to D3 value (only for channel 1 and 2)

D3
- 0 Left channel DAC
- 1 Right channel DAC

For channel 3, D0 to D2 are loaded into the unique DAC.

A1 A0

1 1 When A0, A1 are in this configuration, the value of D0 to D3 causes an increment or a decrement of the content of left/right DAC of a channel. The inc/dec operation and the DAC register selection (right or left) are selected according to the following truth table:

D3	D2	D1	D0
dec LEFT	inc LEFT	dec RIGHT	inc RIGHT

The change in DAC registers is done immediately after receiving the data.The configurations D3, D2 = 11 and D1, D0 = 11 are not allowed. (Them can cause faulty operations) Channel 3 has only one DAC; the change in its value is done according to D0,D1 value.

D1	D0
dec DAC	inc DAC

D1, D0 = 11 is not allowed (they can cause faulty operations).

Output Operation

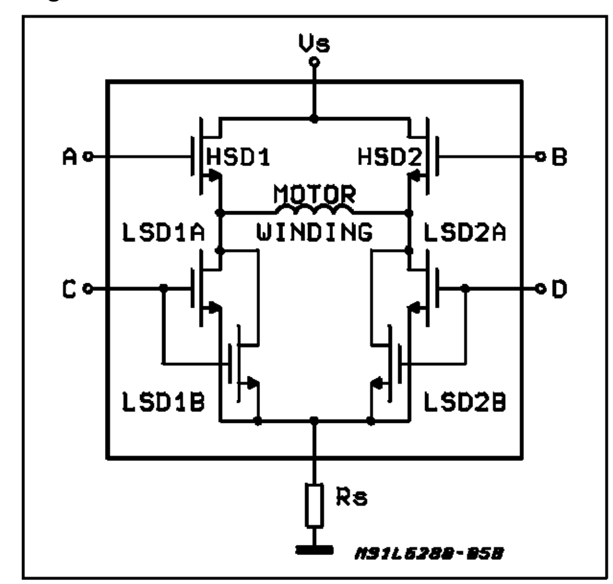
In full bridge and dual half bridge configurations, the output stages will operate according to D1, D2, D3 values.

FULL BRIDGE CONFIGURATION (CH1 and CH2)

In full bridge configuration the cennection between the output of the high side drivers and the corresponding low side drivers has to be made with external jumpers. The output stage diagram here below (Fig. 13) must be substituted inside the blank boxes in the following block diagrams.

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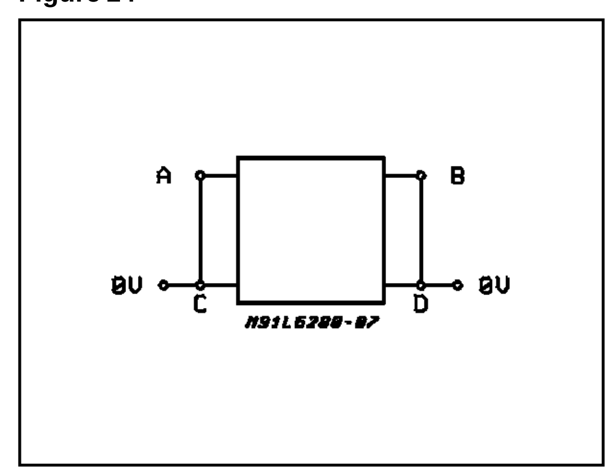
Figure 13



D0	D1	D2	D3	
X	0	0	0	Tristate left and right

All output DMOSs of the channel are OFF (Fig. 14)

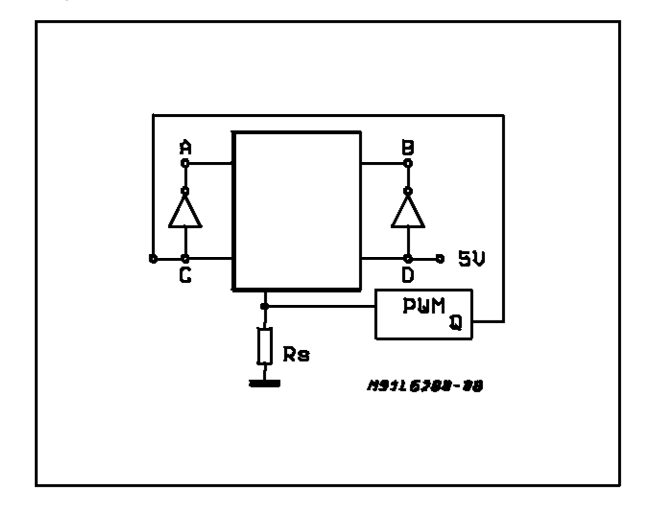
Figure 14



D0	D1	D2	D3	
X	0	0	1	Chopper left side; fixed right side (one phase chopping)

The left side of the bridge is controlled by the PWM loop while HSD2 is held OFF and LSD2A and 2B are held ON. During ON time (Q low) the current flows thrugh HSD1, motor winding and LSD2A and 2B. During OFF time the current can recirculate through LSD1A, 1B, 2A and 2B (Fig. 15)

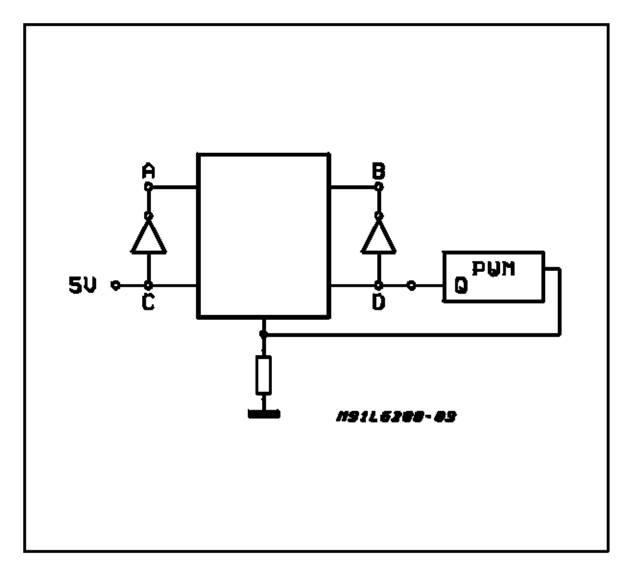
Figure 15



D0	D1	D2	D3	
X	0	1	0	hopper right side, fixed left side (one phase chopping)

As above but with the two channel exchanged each to other (Fig. 16).

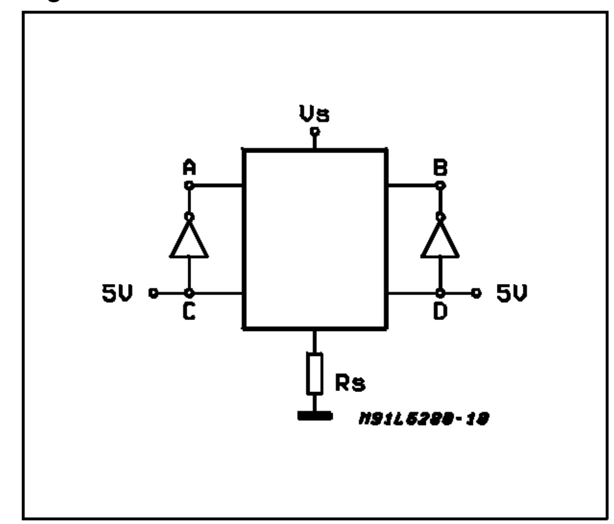
Figure 16



D0	D1	D2	D3	
X	0	1	1	Fixed both left and right (brake action)

All High side drivers are held OFF while all low side drivers are held ON. The motor winding is short circuited through the low side drivers; the motor's back EMF acts as a brake voltage (Fig. 17).

Figure 17



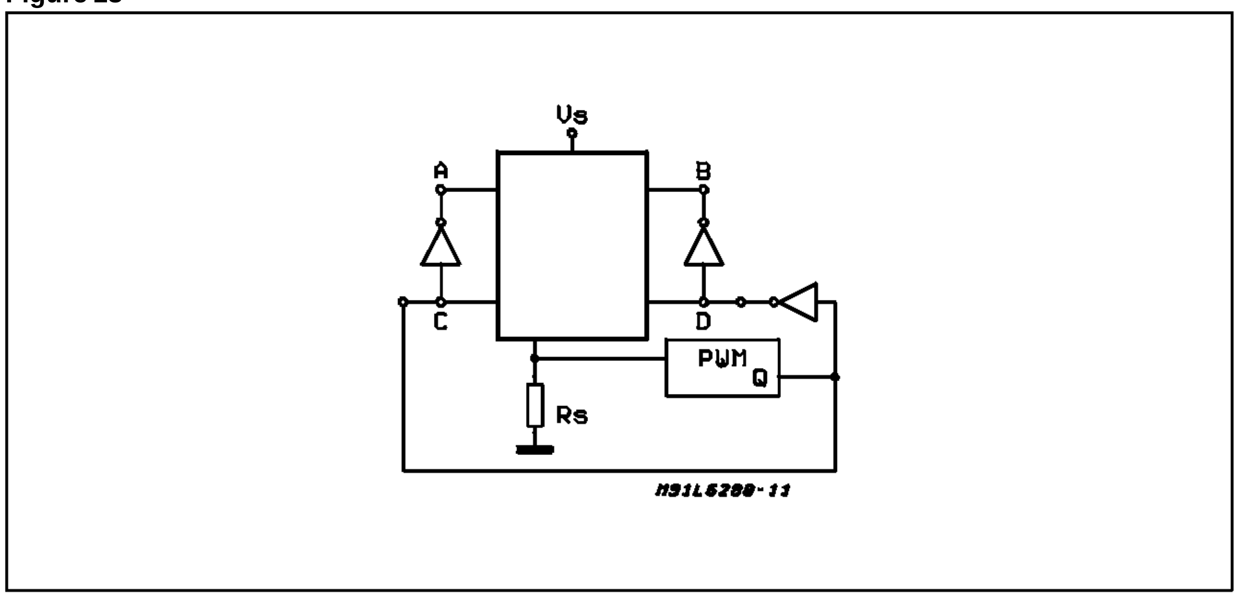
D0	D1	D2	D3	
X	1	0	0	Three state left and right (see X000 configuration)

D0	D1	D2	D3	
X	1	0	1	Diagonal chopper (Two phase chopping)

During

During On time (Q=LOW) the current flows through HSD1, motor winding and LSD2A and 2B. During OFF time (Q = HIGH) the current can recirculate through LSD1A and 1B motor winding and HSD2 (Fig. 18).

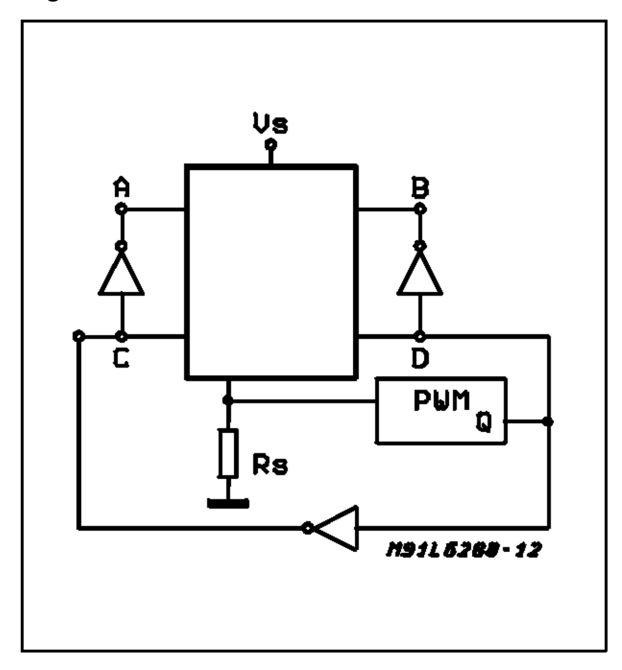
Figure 18



D0 D1 D2 D3 INVERTED DIAGONAL CHOPPER (Two phase chopping)

During ON time (Q = LOW) the current flows through HSD2, motor winding and LSD1A and 1B. During OFF time (Q = HIGH) the current can recirculate through LSD2A and 2B motor windind and HSD1 (Fig.19).

Figure 19

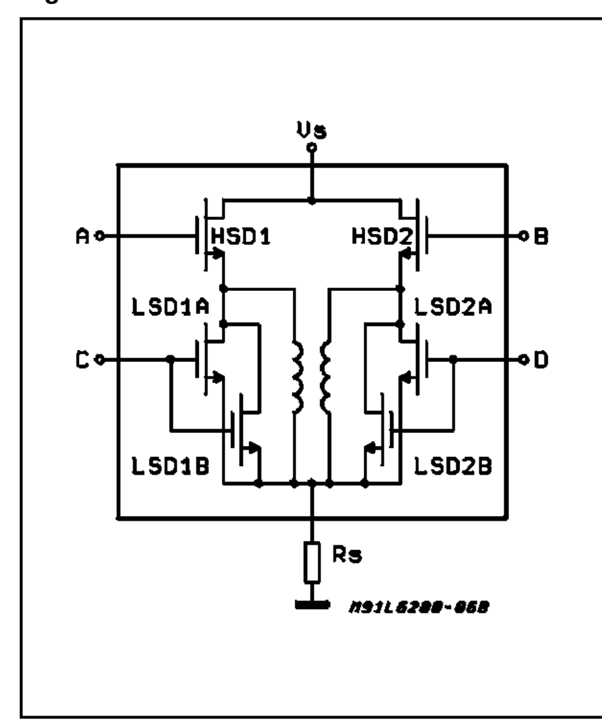


D0	D1	D2	D3	
X	1	1	1	Tristate left and right (see X000 configuration)

DUAL HALF BRIDGE CONFIGURATION (CH1 and CH2)

In dual half bridge configuration the connection between the output of the high side drivers and the corresponding low side drivers has to be made with external jumpers. The output stage block diagram shown in figure 20 must be substituted in side the blank boxes in the following block diagrams. In dual half bridge configuration, the time sharing strategy is always used.

Figure 20

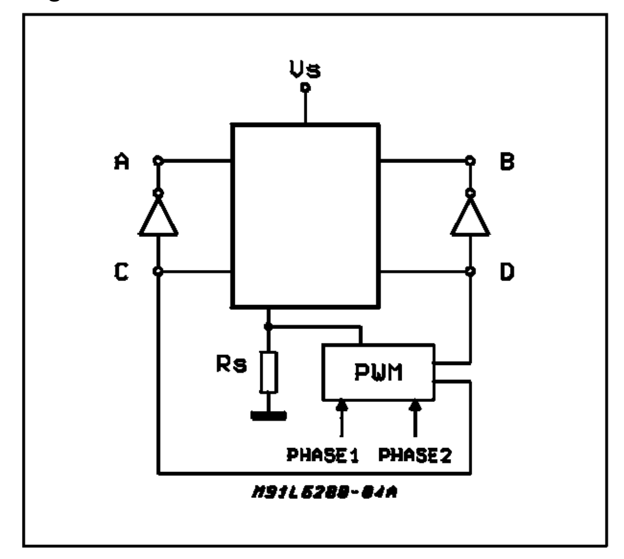


D0	D1	D2	D3	
X	0	0	0	Tristate left and right
X	0	0	1	Chopper left, fixed righ
X	0	1	0	Chopper right, fixed left
X	0	1	1	Fixed left and right. For these configurations, see the corresponding shown in Full Bridge Configuration paragraph (Page 14/24).

D0	D1	D2	D3	
X	1	0	0	Chopper left chopper right

As foreseen when in unipolar motor configuration(see Figure 5), the time sharing strategy is used (see Figure 10), so when the current in left winding is controlled, the current in right winding recirculate trough the low side drivers and not through the sense resistor (Fig. 21).

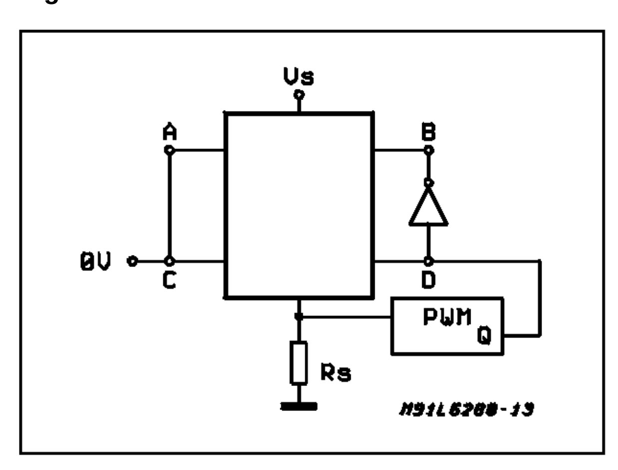
Figure 21



D0	D1	D2	D3	
X	1	0	1	Tristate left, chopper right

During ON time (Q = LOW) the current flows through high side driver HSD2, right winding and sense resistor. During OFF time the current recirculate through winding and side drivers LSD2A and LSD2B (Fig. 22).

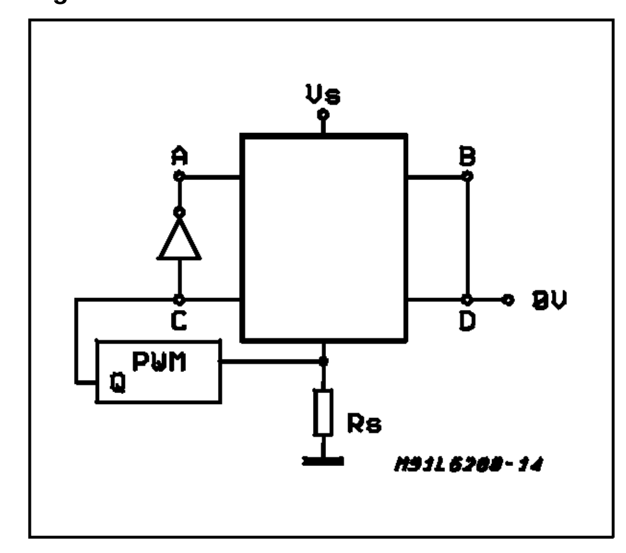
Figure 22



D0	D1	D2	D3	
X	1	1	0	Tristate right, chopper left

During ON time (Q = LOW) the current flows through high side driver HSD1, left winding and sense resistor. During OFF time the current recirculate through the winding and low side drivers LSD1A and LSD2A (Fig 23).

Figure 23



D0	D1	D2	D3	
X	1	1	1	Tristate left and right (see X000 configuration of full bridge).

APPLICATION INFORMATION

An application circuit useful to test the performance of the L6280 can be formed as shown on Figure 24: CH1 drives one unipolar stepper motor, CH2 drives a DC motor, CH3 drives one solenoid and the SMPS can supply continuously 0.5A.

If the Watch Dog and the Chip Select functions are not of interest, pins 22 and 23 must be grounded. Each sensing resistor would be obtained by the parallel of two or more metal film resistor of the same value to minimize their series equivalent inductance.

Generally, optimum stability of the SMPS voltage control loop, is achieved by a series network made by 1nF and 39 KΩ (see pin 15) and by using an output capacitor of 100µF having an equivalent series resistance of 100 mΩ (see pin 14): the most of the unexpensive aluminium electrolithic capacitors can be right.

The snubber network at the secondary winding of the step-down inductor can be saved by accepting a not regulated voltage at the Charge Pump input pin 13. This condition is not recommended when the supply voltage and/or the SMPS output current changes too much (for instance respectively 20V $\pm$ 30% and/or 100 to 800 mA).

The inductance value of the primary winding of T1 defines the peak-to peak current ripple that flows throught itself, that is the minimum output current that allows the correct behaviour in continuous mode of the SMPS; nevertheless, the device is not demaged if it is obliged to work in discontinuous mode at a low current level.

Figure 25 shows the characteristics of the transformer T1 suitable to be used on the Application of Figure 24:

The maximum output current is of 500 mA continuous but current peaks of 800 mA can be sinked out without the risk of the core saturation. To avoid the discontinuous mode, the minimum SMPS output current must be of 70mA. The rectified voltage trend for the high side gate drive at pin 13 is as shown on Figure 26.

Not equally cheap, the choice of a toroidal core for T1 can optimize the application.

Instead of this, another solution can be as in Figure 27a it is shown. This is a full wave rectifier of the voltage at pin 3; Z1 and R1 clamp the positive peak while the forward characteristic of the Zener rectifies the negative peak and charges C1. The recommended Zener voltage is of 12V.

Could happen that the V_{SS} output voltage is not requested because already available: in this case and only if at least one unipolar stepper motor is continuously driven, the solution shown in Figure 27b can be implemented. The step down output components can be left out.

The connection of the network is as follows:

A: to pin 4 (or pin 5) when the unipolar motor is driven via CH1;
to pin 41 (or pin 42) when the unipolar motor is driven via CH2;
B: to pin 1
C: to pin 13

The SMPS switching frequency is the same of the oscillator frequency that can be typically defined by:

$$f_{osc} = \frac{9}{RC}$$

Referring to Fig. 24 it is calculated f_{osc} = 82KHz.

CH3 is chopped at the same frequency. The output diodes must be chosen according to the solenoid working current (50ns of reverse recovery time or better): for a current less than 1 A, the PLQ08 is a good choice.

Driving one unipolar stepper motor, output protection diodes (Transil) are recommended: CH1 in Fig 24 uses four BZW04 - 48 diodes; when a low current motor is driven or a Vs less than 20V is supplied, four fast diodes and only one Zener diode can be used as a protection of the outpus (see Figure 28). The driving of DC motor needs the connection as shown for CH2 (full bridge configuration).

The drive of one bipolar stepper motor by using CH1 and CH2 both in full bridge configuration allows the use of a higher supply voltage level that however cannot exceed the Absolute Maximum

Ratings of 35V:a max value of 33V is reccommended.

In this case, at each couple of outputs for the bipolar windings, a snubber network must be connected. This network is done by the series of a resistor and of one capacitor:

$R_{snub} = V_S$ max/Imotor peak;

C_{snub} = Imotor peak/ (dv/dt)

One dv/dt of 200V/µsec is generally a correct choice.

Of course, care must be taken in the Printed Circuit Board design regarding the ground paths and the high current loops.

An example of P.C.B. layout is shown in Figure 29ab; Figure 30 shows the Schematic Diagram of the circuit of the L6280 S.P.D. S.AB.

The driving signals useful for this board can be easily generated by using an additional board (EMU KIT 512) not described here.

On Figure 29a it can be observed the copper area near the I.C. is used to sink out the heat from the device. Useful thermal characteristics of the L6280 are shown in Figure 31 and 32.

Figure 24: Application Test Circuit of the L6280

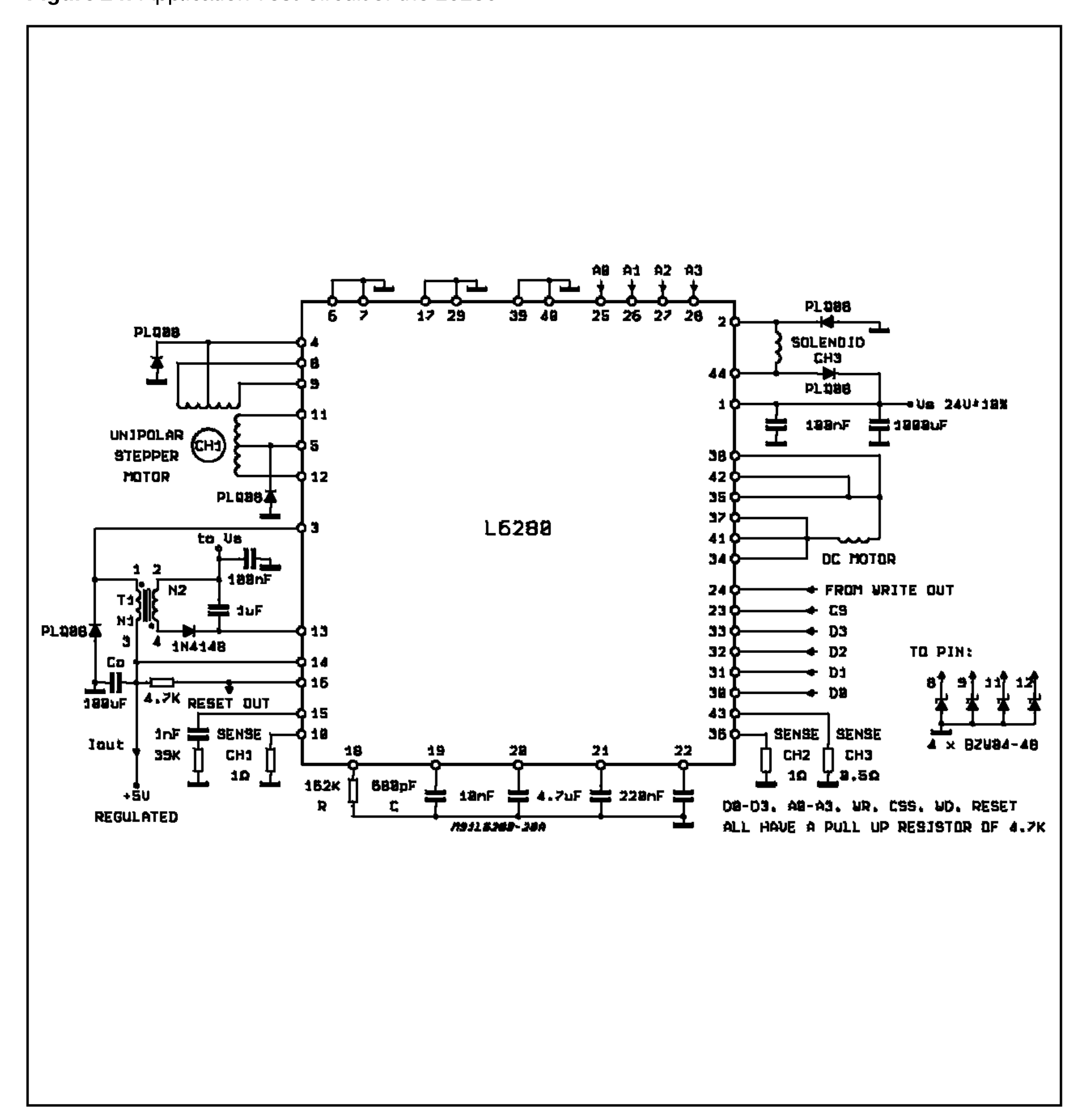
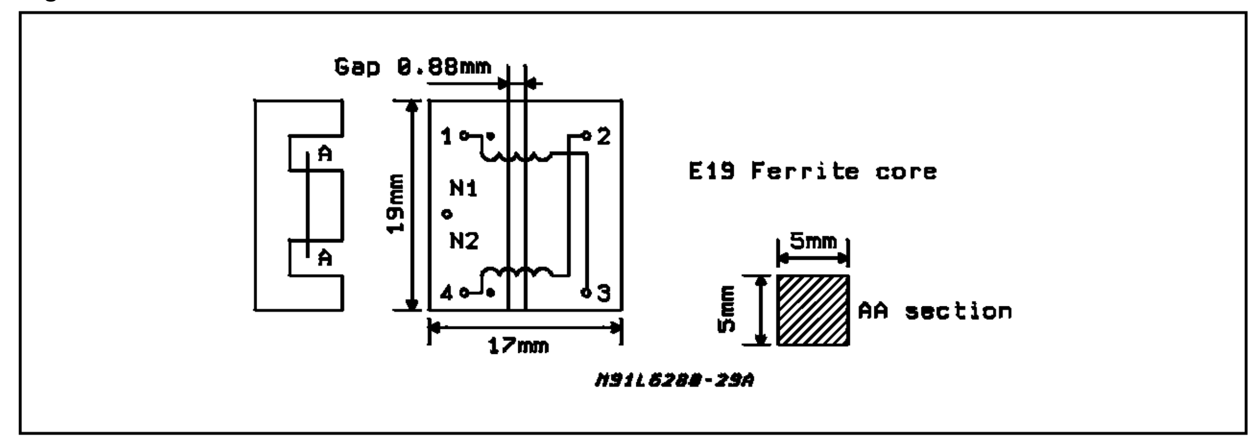


Figure 25: Characteristics of the Transformer T1.



N1: 118 tourns, copper wire ∅ 0.35mm
N2: 88 tourns, copper wire ∅ 0.2mm

TYPICAL PARAMETERS

N1	L_1 = 560µH R_1 = 680mΩ	@ 1KHz
N2	L_2 = 300µH R_2 = 1.5Ω	@ 1KHz

Figure 26: Charge Pump Voltage vs. Supply Voltage by using the transformer shown on Figure 25

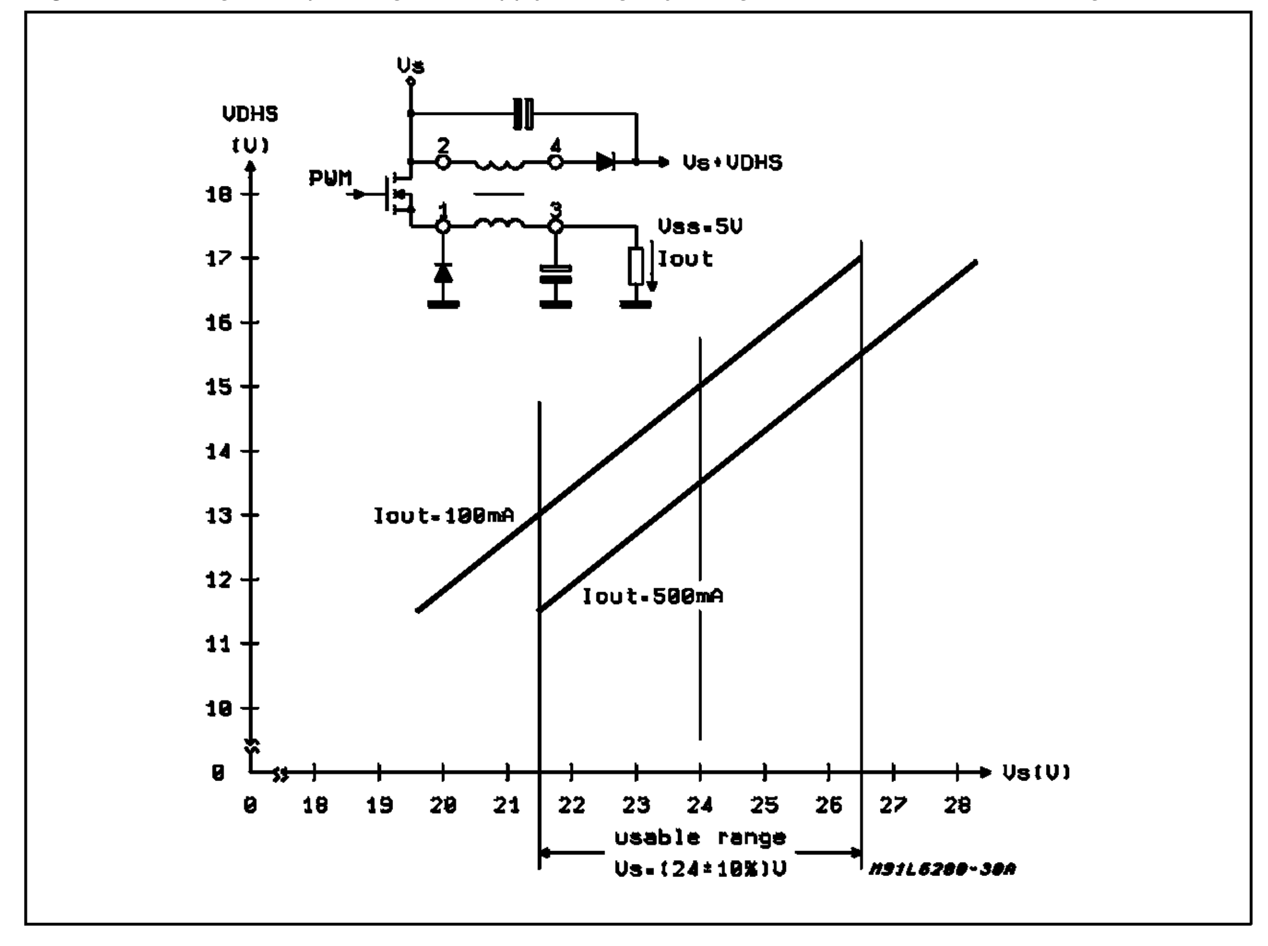


Figure 27a : Other Charge Pump Solution

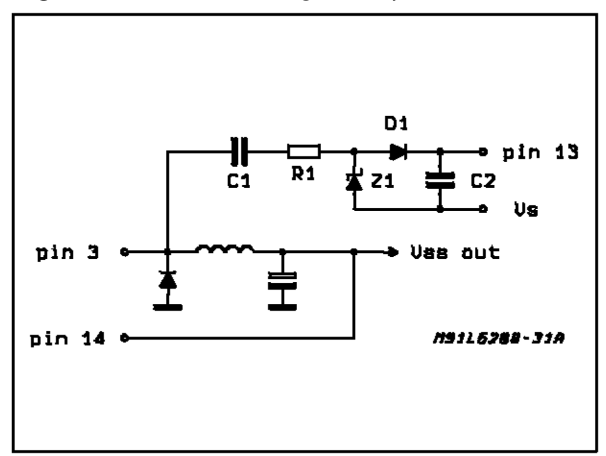


Figure 27b : Other Charge Pump Solution

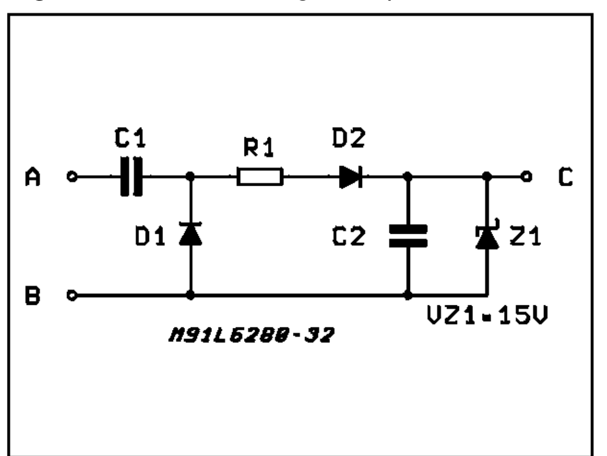


Figure 28 : Unexpensive Output Protection Network for the Unipolar Motor Driving

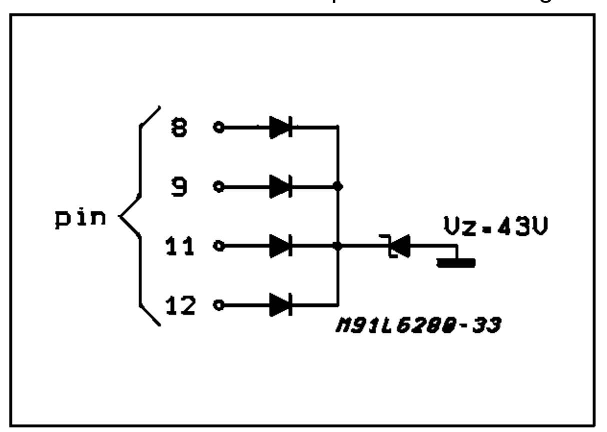


Figure 29a: L6280 PCB Components Side (1st metallization)

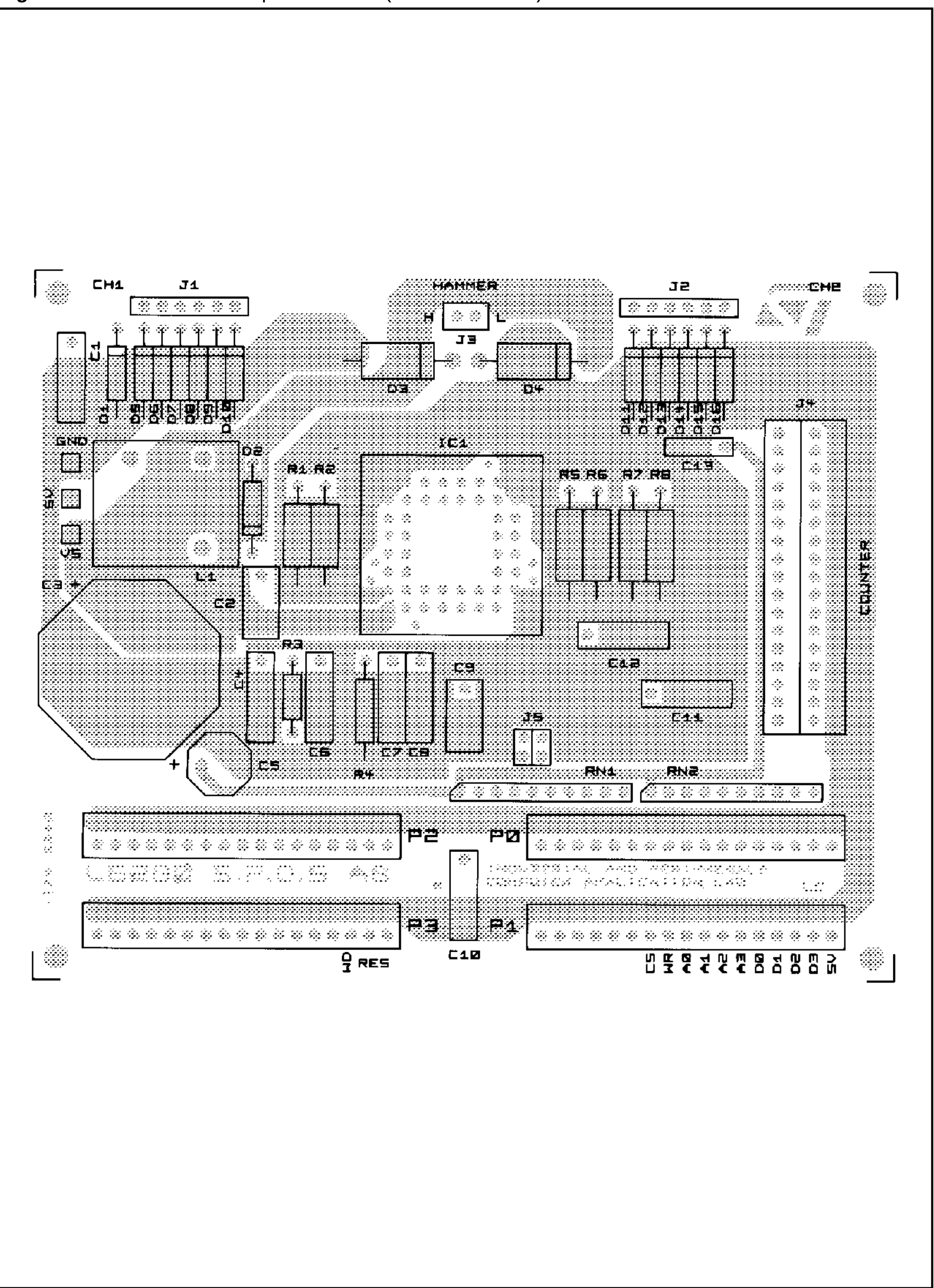


Figure 29b: P.C.B. Back Side (2nd metallization)

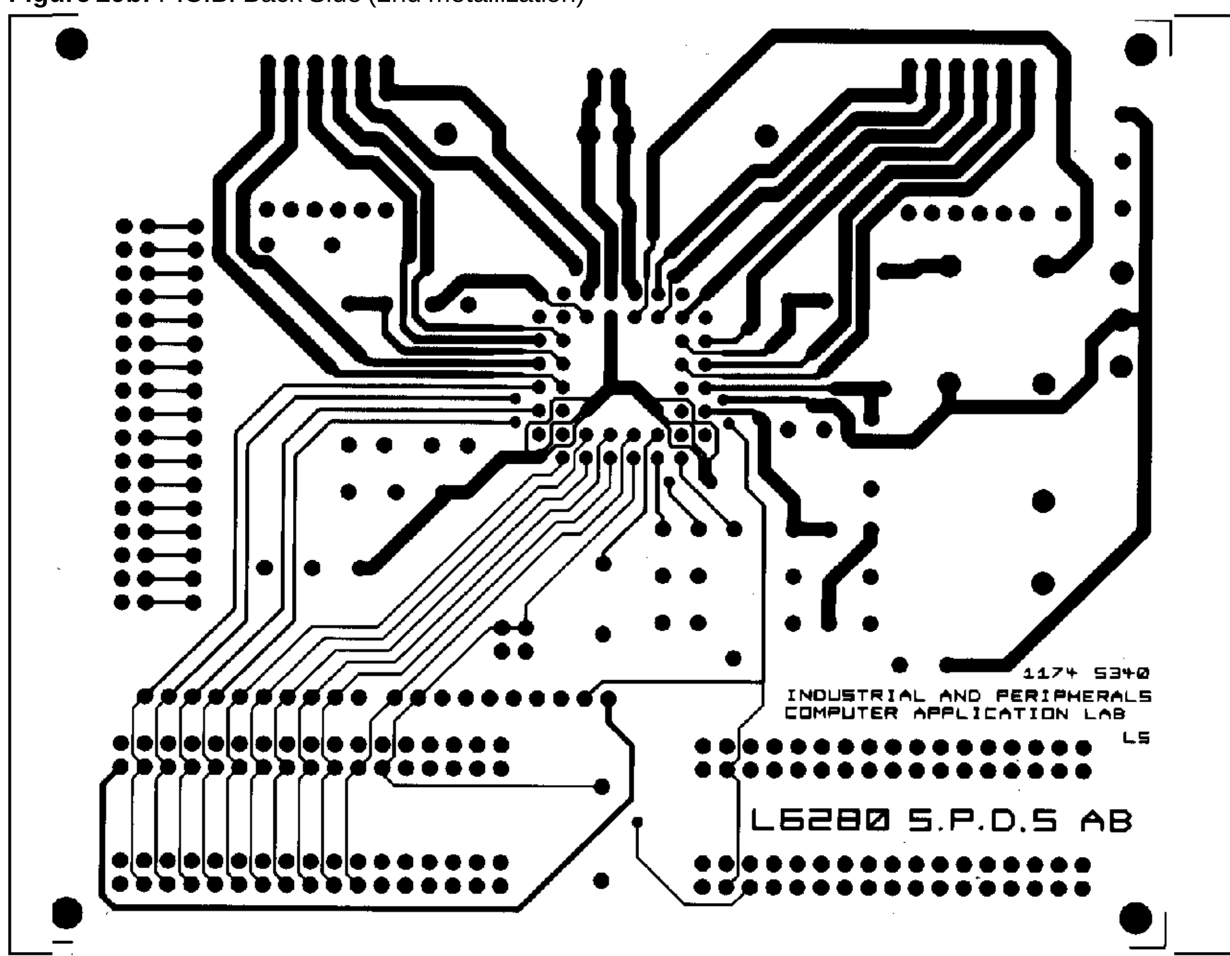


Figure 30: Schematic Diagram of the Circuit Assembled on the L6280-AB (Figure 29)

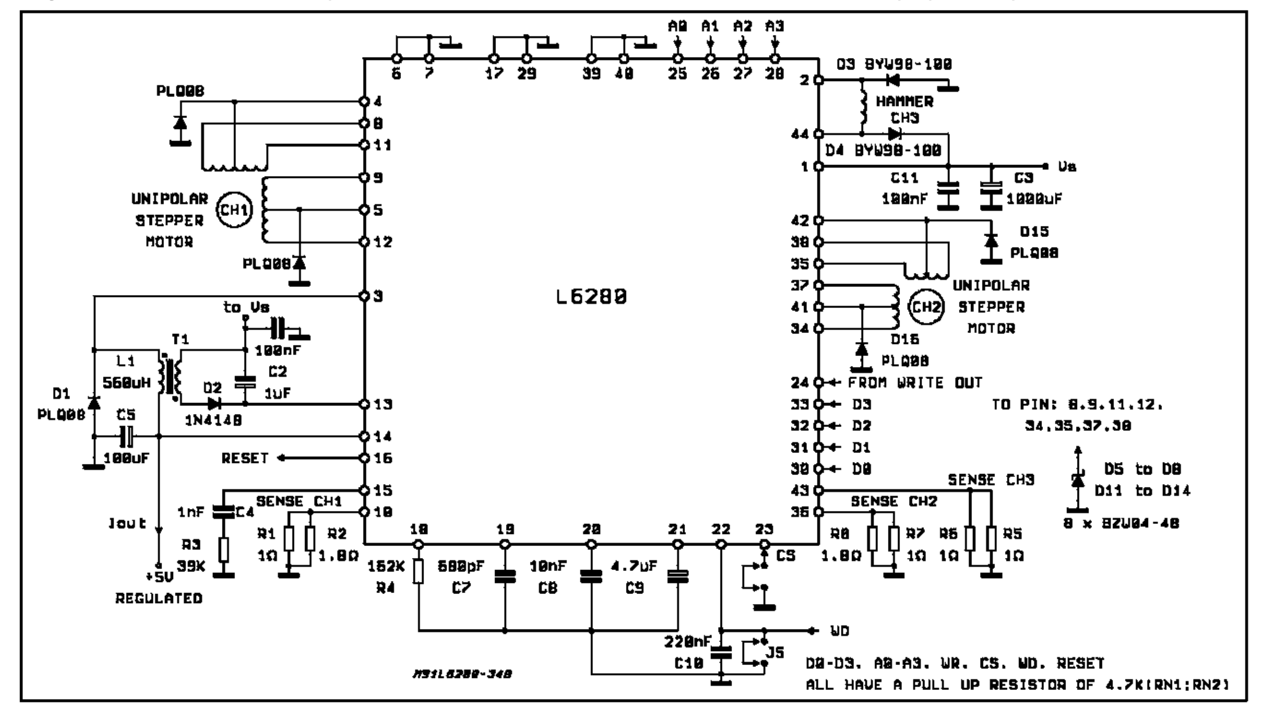


Figure 31; Typical Transient Thermal Resistance vs. Single Pulse Width.

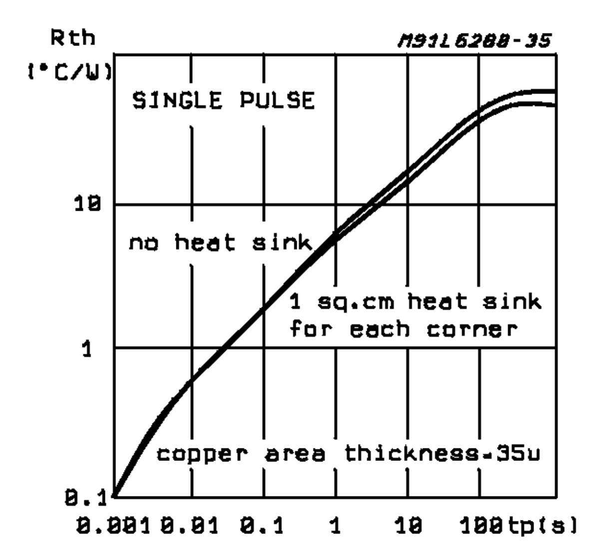
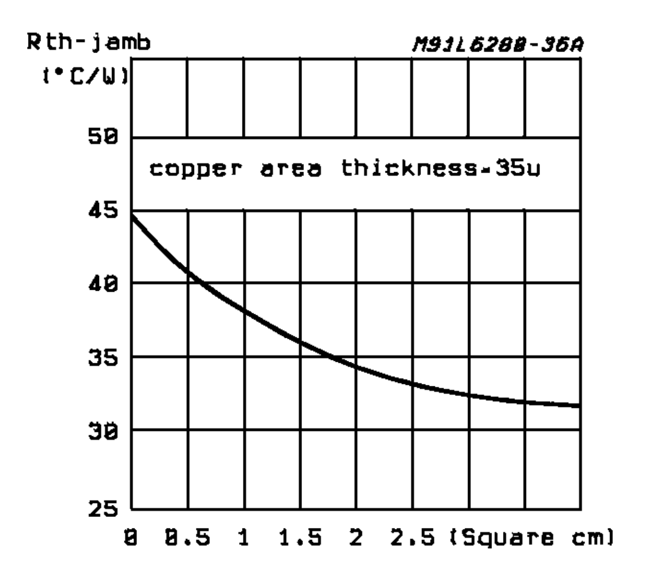
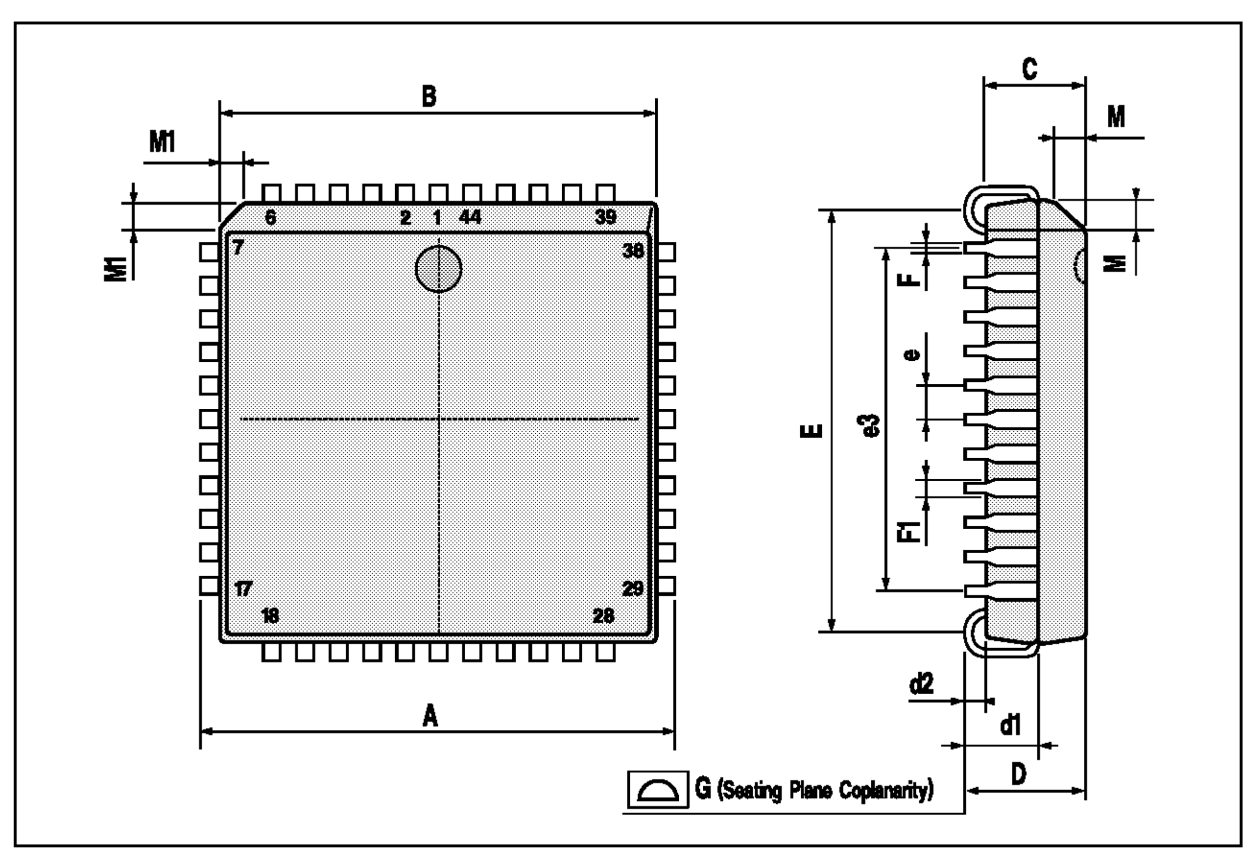


Figure 32; Typical Thermal Resistance vs. Heatsinking Copper Area.



PLCC44 PACKAGE MECHANICAL DATA

DIM.	mm			inch		
	MIN.	TYP.	MAX.	MIN.	TYP.	MAX.
A	17.4		17.65	0.685		0.695
B	16.51		16.65	0.650		0.656
C	3.65		3.7	0.144		0.146
D	4.2		4.57	0.165		0.180
d1	2.59		2.74	0.102		0.108
d2		0.68			0.027	
E	14.99		16	0.590		0.630
e		1.27			0.050	
e3		12.7			0.500	
F		0.46			0.018	
F1		0.71			0.028	
G			0.101			0.004
M		1.16			0.046	
M1		1.14			0.045	



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